AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A multilayer semiconductor device assembly jig for minimizing the displacement of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process, comprising:

a lateral position restriction mechanism for positioning and aligning a plurality of stacked semiconductor modules on a solid base member with their respective lateral positions mutually restricted;

a removable height restriction mechanism disposed opposite said base member and which interfaces with said lateral position restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member and which is removed prior to mounting the jig onto a mother substrate;

a mother substrate alignment mechanism for providing alignment with reference to a the mother substrate on which the jig will be mounted; and

further wherein each of the plurality of semiconductor modules is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

2. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 1, wherein said lateral position restriction mechanism comprises ~~comprising~~ a box-shaped member formed from two pairs of opposing side walls formed in a rectangular shape and which is positioned on said base member and ~~having~~ and which has a storage space for storing said semiconductor modules in a layered state,

wherein an inner wall surface of said storage space constitutes said lateral position restriction mechanism.

3. (Original) The multilayer semiconductor device assembly jig according to claim 2, wherein said alignment mechanism comprises a plurality of positioning pins and positioning holes for receiving the positioning pins which are correspondingly formed in said box-shaped member and said mother substrate.

4. (Original) The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which are used for securing at least three different portions of an outer periphery of said semiconductor modules.

5. (Previously Presented) The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of

positioning pins secured in said base member and which pierce through positioning holes formed in said semiconductor modules.

6. (Previously Presented) The multilayer semiconductor device assembly jig according to claim 5, wherein said positioning pins also pierce through a positioning hole formed in said mother substrate when the jig is mounted on the mother substrate.

7. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism ~~further~~ comprises:

a cover member secured over said semiconductor modules.

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Currently Amended) A multilayer semiconductor device assembly jig for minimizing the displacement of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process, comprising:

a lateral position restriction mechanism for positioning and aligning a plurality of stacked semiconductor modules on a solid base member with their respective lateral positions mutually restricted, the lateral position restriction mechanism comprised of two opposed side walls having a single stack of the semiconductor modules therebetween;

a removable height restriction mechanism disposed opposite said base member and which interfaces with said lateral position restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member, said height restriction mechanism being located directly above the stacked semiconductor modules and wherein said height restriction mechanism is removed prior to mounting the jig on a mother substrate;

a mother substrate alignment mechanism for providing alignment with reference to a the mother substrate on which the jig will be mounted;

and further wherein each of the plurality of semiconductor modules is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

12. (Previously Presented) The multilayer semiconductor device assembly jig of claim 11, wherein the alignment mechanism is comprised of a plurality of vertical pins arranged adjacent and in contact with sides of the stacked semiconductor modules.

13. (Previously Presented) The multilayer semiconductor device assembly jig of claim 11, wherein the alignment mechanism is comprised of a plurality of vertical pins that extend through the stacked semiconductor modules.

14. (Currently Amended) An assembly jig for minimizing the displacement of a plurality of semiconductor modules disposed within the assembly jig during a manufacturing process ~~a semiconductor module~~ comprising:

two pairs of substantially parallel opposed side walls formed on a solid base member;

a removable cover member located opposite said base member and which interfaces with ~~over~~ the side walls;

a plurality of semiconductor modules stacked and surrounded by the side walls such that the modules are aligned and their lateral motion is prevented by the side walls, wherein the semiconductor modules are comprised of at least one chip and one wiring board;

and further wherein the removable cover member is positioned such that it prevents vertical displacement of an uppermost semiconductor module.

15. (Previously Presented) The assembly jig of claim 15 wherein pins extend through portions of the cover member and the side walls.

16. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 1, wherein when the height restriction mechanism is removed and the jig is mounted on

the mother substrate, a bottom-most one of the stacked semiconductor modules is caused to come into electrical contact with the mother substrate.

17. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 11, wherein when the height restriction mechanism is removed and the jig is mounted on the mother substrate, a bottom-most one of the stacked semiconductor modules is caused to come into electrical contact with the mother substrate.

18. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 14, wherein when the height restriction mechanism is removed and the jig is mounted on ~~the~~ a mother substrate, a bottom-most one of the stacked semiconductor modules is caused to come into electrical contact with the mother substrate.

19. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 1, wherein said ~~device functions~~ height and lateral position restriction mechanisms function to limit a deformation of the semiconductor modules during ~~a subsequent~~ the manufacturing process.

20. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 1, wherein said ~~device functions to maintain a specified height of the plurality of stacked semiconductor modules during a subsequent manufacturing process~~

said mother substrate alignment mechanism is formed in said lateral position restriction mechanism.

21. (Cancelled)